ROHS

PRODUCT SPECIFICATION

128*64 DOTS LCD MODULE
MODEL: G1206ZDTRNFG-B1 Ver:1.4

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER'S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY
2017.3.15			邱信隆

Revision Status

Version	Revise Date	Page	Content	Modified By
Ver 1.0	2015-12-09		First Issued	
Ver 1.1	2016-02-01	4	Update General Description	
Ver 1.2	2016-10-10	4,10	Update Sample NO.; Update IDD;	
Ver 1.3	2016-11-07	12~14	Add COMMAND TABLE;	
Ver 1.4	2017-03-15	4	Update Sample NO.;	

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1. Technology Description

BCD (Bi-stable Cholesteric Display) is a sunlight readable reflective LCD with extremely low power consumption characteristics. Due to the non-volatile memory feature of the technology, zero power is required to retain the image of the display. Energy is only required to change the displayed image. No backlighting is required, only ambient lighting from the surrounding is required. Readability when under direct sunlight is excellent and good contrast from viewing at very wide angles are possible.

2. Typical Applications

This module is intended for general purpose graphic and character display applications. Suggested uses include instrumentation, remote control, electronic product or price label, point of sale display, general purpose indoor or outdoor signage and information display.

3. General Description

The features of LCD are as follows

* Passive matrix bistable cholesteric LCD graphic module
* Color : Blue & White
* Display Type :VA
* Driver/Controller IC :SSD1603
* Interface Input Data : 4-wires Serial Interface
* Driving scheme : Special BCD driving scheme
* Driving Method : 1/64 Duty,static
* Viewing Direction : Full Viewing
* Backlight : Without
* Polarizer Mode : Without polarizer
  White character with Blue background

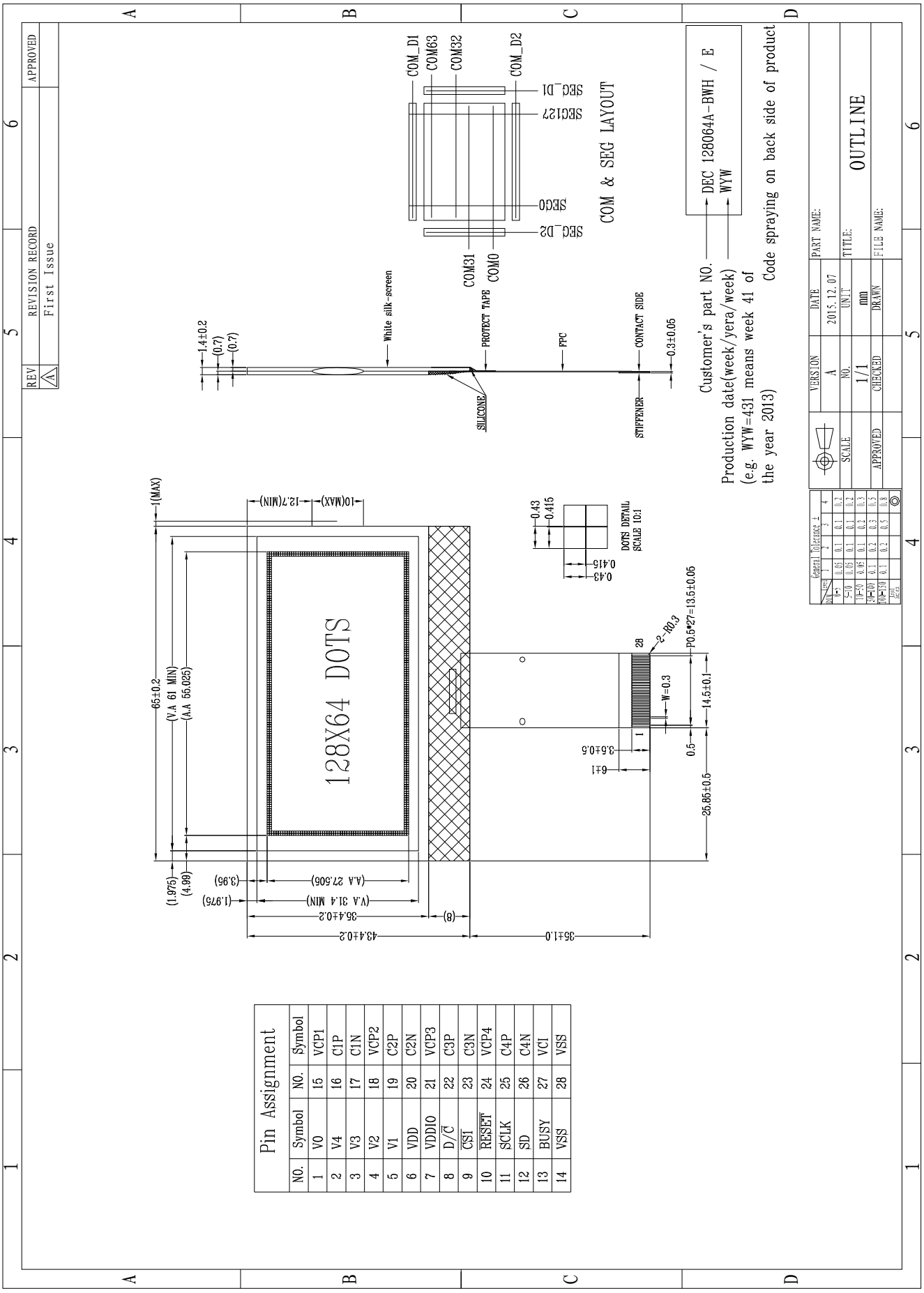
*Sample NO. : G1206ZDTRNFG-B1_03/20170308

4. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Item	Specification	Unit
Module Size	65(W) x 43.4(H) x 1.4(D)	mm
Active Area	55.025(W) x 27.505(H)	mm
Viewing Area	61 MIN(W) x31.4 MIN(H)	mm
Number of Dots	128 X64 Dots	-
Dot Size	0.415(W) x 0.415(H)	mm
Dot pitch	0.43(W) x 0.43(H)	mm



Pin Assignment			
NO.	Symbol	NO.	Symbol
1	V0	15	VCP1
2	V4	16	C1P
3	V3	17	C1N
4	V2	18	VCP2
5	V1	19	C2P
6	VDD	20	C2N
7	VDDIO	21	VCP3
8	D/$\overline{C}$	22	C3P
9	$\overline{CS1}$	23	C3N
10	$\overline{RESET}$	24	VCP4
11	SCLK	25	C4P
12	SD	26	C4N
13	BUSY	27	VCI
14	VSS	28	VSS

Figure 1: Module Specification

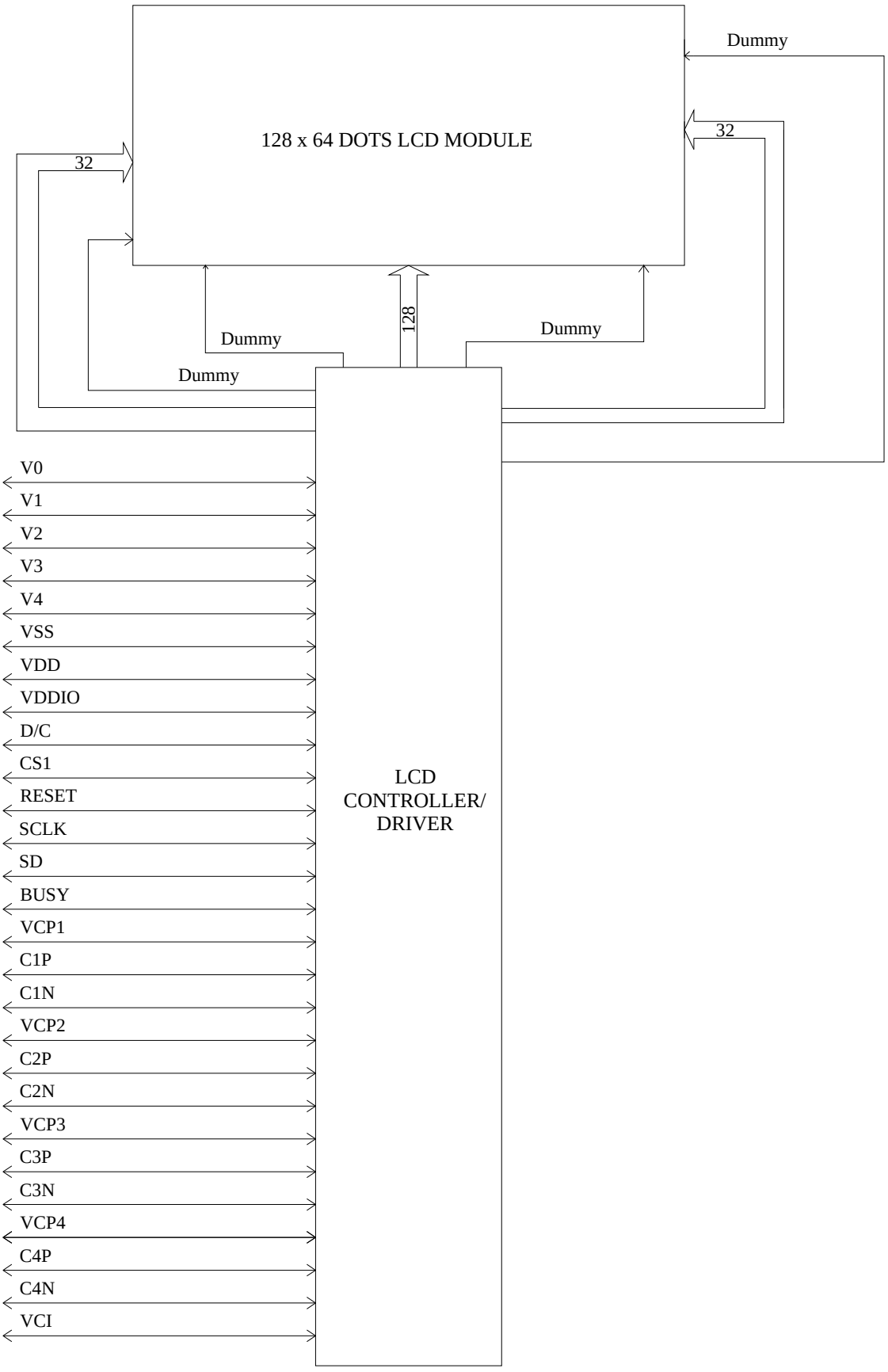
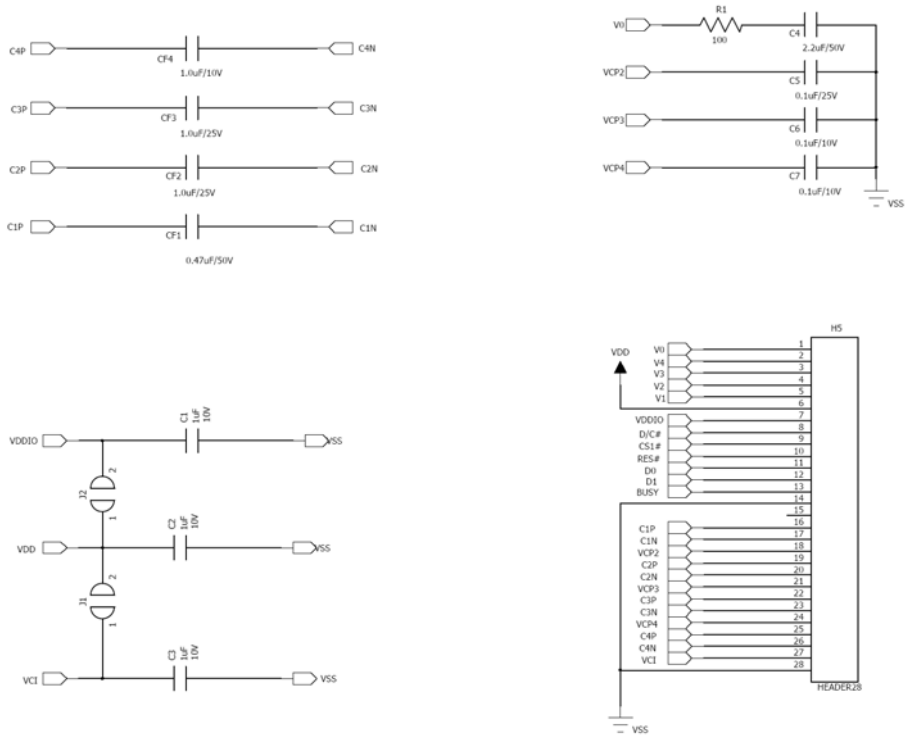


Figure 2: Block Diagram



COG Version IC Interface

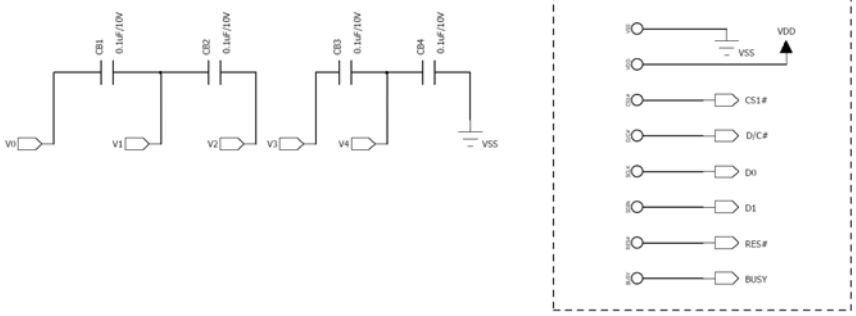


Figure 3: Circuit Diagram

5. Interface Signals

Table 2

PIN NO.	SYMBOL	FUNCIONS
1	V0	It is the high voltage power input pin and panel driving voltage. It should be connected to VCP1.
2	V4	Panel driving voltage. If bias divider is enabled with the presence of V0. The voltage is equal to 1/N * V0, where N is equal to the Bias ratio Setting.
3	V3	Panel driving voltage. If bias divider is enabled with the presence of V0. The voltage is equal to 2/N * V0, where N is equal to the Bias ratio Setting.
4	V2	Panel driving voltage. If bias divider is enabled with the presence of V0. The voltage is equal to (N-2)/N * V0, where N is equal to the Bias ratio Setting.
5	V1	Panel driving voltage. If bias divider is enabled with the presence of V0. The voltage is equal to (N-1)/N * V0, where N is equal to the Bias ratio Setting.
6	VDD	This pin is the system power supply pin of the logic block.
7	VDDIO	Power supply for interface logic level. It should be match with the MCU interface voltage level. It must always be equal or lower than VDD.
8	D/C	This pin is Data/Command control pin. A high at D/C indicates data input while a low at D/C indicates command input.
9	CS1	These pins are the chip select inputs for communication between MCU. To select the chip CS1# must be low and CS2 must set high. For serial mode, it is needed to select the chip which CS1# must be low and CS2 must set high.
10	RESET	This pin is the reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for reset sequence is 20us.
11	SCLK	In serial interface mode, D1 is the serial data input (SDIN), D0 is the serial clock input, (SCLK).
12	SD	
13	BUSY	A high level indicates busy status (output driving waveform) of the driver.
14	VSS	Ground.
15	VCP1	DC/DC output voltage. Connect with a capacitor to VSSC. It should be connected to V0.
16	C1P	DC/DC flying capacitor terminal. Connect a capacitor between C1N and C1P.
17	C1N	
18	VCP2	DC/DC intermediate output voltage. Connect with a capacitor to VSSC. If using external mode with HV buffer enabled, it should be connected to V0.
19	C2P	DC/DC flying capacitor terminal. Connect a capacitor between C2N and C2P.
20	C2N	
21	VCP3	DC/DC intermediate output voltage. Connect with a capacitor to VSSC.
22	C3P	DC/DC flying capacitor terminal. Connect a capacitor between C3N and C3P.
23	C3N	
24	VCP4	DC/DC intermediate output voltage. Connect with a capacitor to VSSC.
25	C4P	DC/DC flying capacitor terminal. Connect a capacitor between C4N and C4P.
26	C4N	
27	VCI	Power supply for DC-DC converter and analog part of the chip. It should be connected to VDD.
28	VSS	Ground.

6. Absolute Maximum Ratings

6.1 Electrical Maximum Ratings-For IC Only

Table3

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_{DD}	TA=+25℃, Referenced to V_{SS} = 0V	-0.3	+3.6	V
	V_{DDIO}		-0.3	Min(VDD+0.5,+3.6)	V
	V_0		-0.3	+38	V
	V_{CI}		-0.3	+3.6	V
Input Voltage	V_{in}		V_{ss} - 0.3	V_{DDIO} + 0.3	V

Note1: TA = +25℃.

Note2: The maximum applicable voltage on any pin with respect to VSS (0V).

Note3: The modules may be destroyed if they are used beyond the absolute maximum ratings.

6.2 Environmental Condition

Table4

Item	Operating temperature (Topr)		Storage temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-20◦C	+70◦C	-30◦C	+80◦C	Dry
Humidity	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Packing vibration(GB/T5170.14-2009)	Frequency range:10Hz~50Hz Acceleration of gravity:5G X,Y,Z 30 min for each direction.				3 directions

Note : Product cannot sustain at extreme storage conditions for long time.

7. Electrical Specifications

7.1 Typical Electrical Characteristics

At Ta = 25 ˚C, VDD = +3.0V± 5%, VSS=0V.

Table5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (System)	VDD-VSS		-	3.0	-	V
	VCI-VSS		VDD	-	3.5	V
	VLCD		-	24	-	V
Input signal voltage low	V_{IL}		0	-	$0.2V_{DDIO}$	V
Input signal voltage high	V_{IH}		$0.8V_{DDIO}$	-	V_{DDIO}	V
Supply current	IDD	VDD=3.0V	-	0.5	-	mA
	ICI	VCI=3.0V	-	0.9	2.0	mA

* Internally Generated

7.2 TIMING Specifications

At Ta = +25 ˚C, VDD = VCI = VDDIO = +3.0V ± 5%

Table 6

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	60	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
T_{CLKL}	Clock Low Time	30	-	-	ns
T_{CLKH}	Clock High Time	30	-	-	ns
t_{CSS}	Chip Select Setup Time (for D7 input)	30	- -	- -	ns
t_{CSH}	Chip Select Hold Time (for D0 input)	30	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

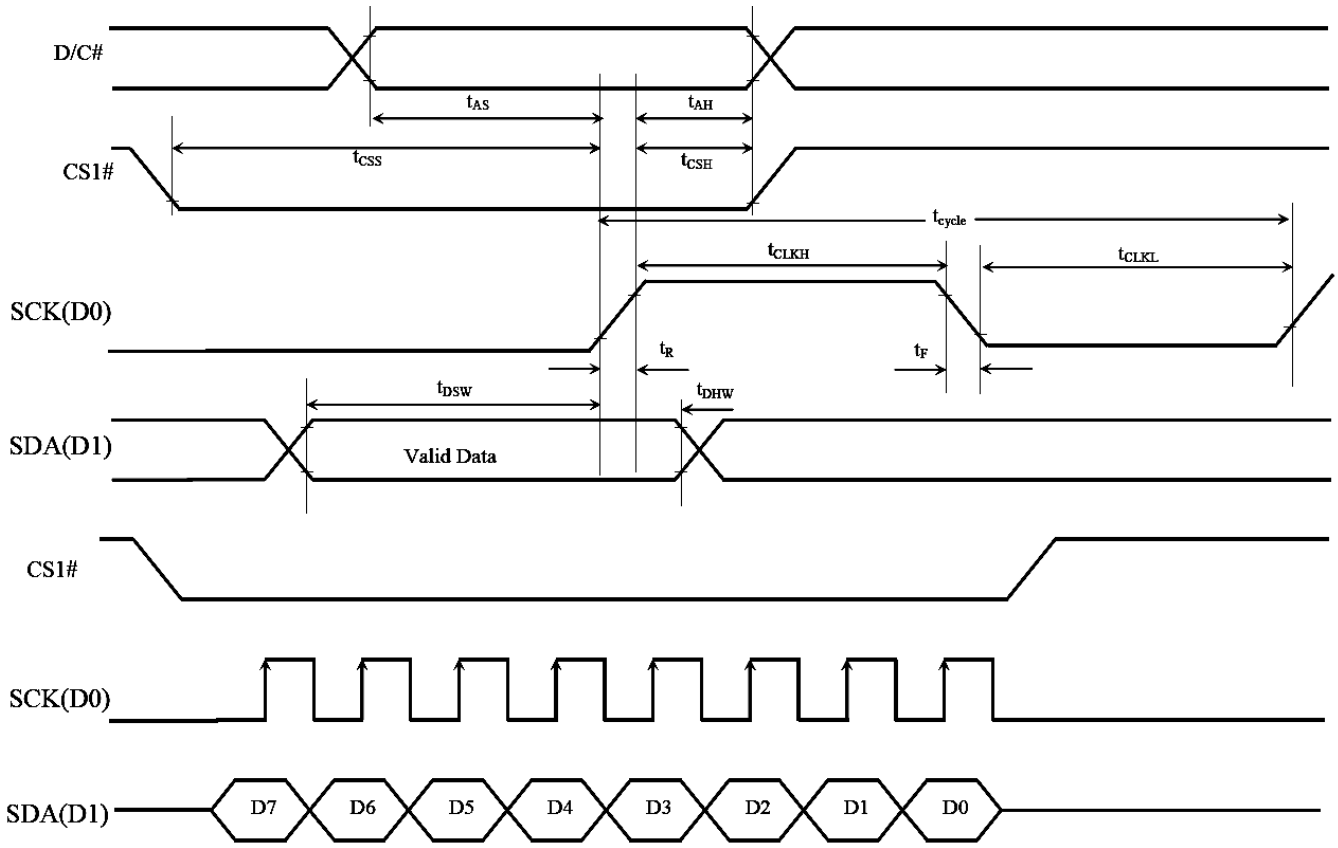


Figure 4:Timing characteristic of 4-wires Serial Interface

7.3 COMMAND TABLE

7.3.1. Command Table

(D/C# = 0, R/W#(WR#) = 0, E=1(RD# = 1) unless specific setting is stated)

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0	10 – 1F	0	0	0	1	A_3	A_2	A_1	A_0	Set column address	Set the higher nibble of the column address register using $A_3A_2A_1A_0$ as data bits. The higher nibble of column address is reset to 0000b after POR. [POR=10_{HEX}] Set the lower nibble of the column address register using $B_3B_2B_1B_0$ as data bits. The lower nibble of column address is reset to 0000b after POR. [POR=00_{HEX}]
0		0	0	0	0	B_3	B_2	B_1	B_0		
0	2A – 2F	0	0	1	0	1	X_2	1	X_0	Set Power Control Register	X_2=0: turns off Charge Pump X_2=1: turns on Charge Pump X_0= 0: turns off Bias Voltage buffer X_0=1: turns on Bias Voltage buffer [POR=$2A_{HEX}$]
0	31	0	0	1	1	0	0	0	1	Driving update	Update RAM content to the screen through segment and common pins. Driving sequence is always in: VA clearing phase →Idle 1 phase → AA clearing phase → Idle 2 phase → Driving phase
0	32	0	0	1	1	0	0	1	0	Driving Scheme	Driving Scheme Setting Active Area Control after clearing X_6X_5 =01, Active Area is responsible to data 1 X_6X_5 =11, Active Area is responsible to data 0 Border Control after clearing X_4 =X_1 =0, Border is responsible to data 0 X_4 =X_1 =1, Border is responsible to data 1 X_3: driving polarity 0: M starts as 1 at Driving phase 1: M starts as 0 at Driving phase X_2: clearing polarity 0: M starts as 1 at Clearing phase 1: M starts as 0 at Clearing phase [POR=00_{HEX}]
0		0	X_6	X_5	X_4	X_3	X_2	X_1	0		
0	40 – 7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Display start line register is reset to 000000 after POR for all MUX modes. [POR=40_{HEX}]
0	80	1	0	0	0	0	0	0	0	Set the control scheme	Set the control scheme. B[4:0] : VA Clearing Duration C[4:0] : Idle 1 Duration D[4:0] : AA Clearing Duration E[4:0] : Idle 2 Duration F[4:0] : Driving Duration G[6:1] : Clearing Voltage H[6:1] : Driving Voltage
0	00	0	0	0	0	0	0	0	0		
0	B[4:0]	0	0	0	B_4	B_3	B_2	B_1	B_0		
0	C[4:0]	0	0	0	C_4	C_3	C_2	C_1	C_0		
0	D[4:0]	0	0	0	D_4	D_3	D_2	D_1	D_0		
0	E[4:0]	0	0	0	E_4	E_3	E_2	E_1	E_0		
0	F[4:0]	0	0	0	F_4	F_3	F_2	F_1	F_0		
0	G[6:1]	0	G_6	G_5	G_4	G_3	G_2	G_1	0		
0	H[6:1]	0	H_6	H_5	H_4	H_3	H_2	H_1	0		
0	93	1	0	0	1	0	0	1	1	Set view area phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If VA clearing phase repeat time is set to 0, it is also needed to set the idle 1 phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	94	1	0	0	1	0	1	0	0	Set idle 1 phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If Idle 1 phase repeat time is set to 0, it is also needed to set the VA clearing phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	95	1	0	0	1	0	1	0	1	Set active area clearing phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If AA clearing phase repeat time is set to 0, it is also needed to set the idle2 phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	96	1	0	0	1	0	1	1	0	Set idle 2 phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting *Remark: If Idle 2 phase repeat time is set to 0, it is also needed to set the AA clearing phase repeat time to 0. [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	97	1	0	0	1	0	1	1	1	Set drive phase repeat times	$X_3X_2X_1X_0$ is Repeat time setting [POR=01_{HEX}]
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	A0 – A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X_0=0: Column address 00h is mapped to SEG0 X_0=1: Column address 83h is mapped to SEG0 [POR=$A0_{HEX}$]

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0 0	A2	1 0	0 0	1 0	0 0	0 0	0 X_2	1 X_1	0 X_0	Set LCD Bias	$X_2X_1X_0$=000: 1/9 $X_2X_1X_0$=001: 1/8, $X_2X_1X_0$=010: 1/7, $X_2X_1X_0$=011: 1/6, $X_2X_1X_0$=100: 1/5, $X_2X_1X_0$=111: 1/4 [POR=00_{HEX}]
0 0	A3	1 0	0 0	1 0	0 X_4	0 X_3	0 0	1 X_1	1 0	Set analog control	X_4X_3 = 00: Disable X_4X_3 = 11: Enable X_1 = 0: Standard BIAS VOLTAGE Buffer Setting X_1 = 1: Extra BIAS VOLTAGE Buffer Setting [POR=00_{HEX}]
0	A4 – A5	1	0	1	0	0	1	0	X_0	Set Entire Display On/Off	X_0=0: normal display X_0=1: entire display on [POR=$A4_{HEX}$]
0	A6 – A7	1	0	1	0	0	1	1	X_0	Set Normal/Reverse Display	X_0=0: normal display X_0=1: reverse display [POR=$A6_{HEX}$]
0 0	A8	1 0	0 X_6	1 X_5	0 X_4	1 X_3	0 X_2	0 X_1	0 X_0	Set Multiplex Ratio	To select multiplex ratio N MUX $X_6X_5X_4X_3X_2X_1X_0$ = N from 2 to 64 [POR=40_{HEX}]
0 0	A9	1 0	0 0	1 0	0 0	1 0	0 0	0 0	1 X_0	Analog Control Auto ON/OFF	X_0= 0: OFF X_0= 1: ON [POR=00_{HEX}]
0 0	AD	1 0	0 0	1 0	0 0	1 0	1 0	0 0	1 X_0	RAM Read/Write Direction	X_0= 0: RAM read/write horizontal X_0= 1: RAM read/write vertical [POR=00_{HEX}]
0 0	AE	1 0	0 X_6	1 X_5	0 X_4	1 X_3	1 X_2	1 X_1	0 X_0	Set Auto Charge pump Threshold Value	$X_6X_5X_4X_3X_2X_1X_0$: Auto Charge Pump Threshold If contrast setting > threshold, 16X Charge Pump setting would be selected, Otherwise, 8X Charge Pump is used. [POR=20_{HEX}]
0	B0 – B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Address	Set GDDRAM Page Address (0-7) for read/write using $X_2X_1X_0$ [POR=$B0_{HEX}$]
0	C0 / C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	X_3=0: normal mode X_3=1: remapped mode COM0 to COM [N-1] becomes COM [N-1] to COM0 when Multiplex ratio is equal to N. [POR=$C0_{HEX}$]
0 0	D3	1 0	1 0	0 X_5	1 X_4	0 X_3	0 X_2	1 X_1	1 X_0	Set Display Offset	After setting MUX ratio less than default value, data will be displayed at the beginning/towards the end of display matrix. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = Y – L Note: max value of L = Y – display MUX Y represents POR default MUX [POR=00_{HEX}]
0 0	E2	1 1	1 1	1 1	0 0	0 0	0 0	1 1	0 1	Software Reset	Initialize internal status registers.
0	E3	1	1	1	0	0	0	1	1	NOP	No operation
0 0	E9	1 X_7	1 0	1 0	0 0	1 0	0 1	0 0	1 0	Set Bias Resistor Ladder	X_7= 0: Disable X_7= 1: Enable [POR=04_{HEX}]
0 0	F6	1 0	1 X_6	1 0	1 0	0 0	1 0	1 0	0 0	Set Internal Oscillator	X_6= 0: Disable X_6= 1: Enable [POR=00_{HEX}]
0 0	FD	1 0	1 0	1 0	1 1	1 0	1 X_2	0 1	1 0	Lock/unlock driver	X_2= 0: unlock driver X_2= 1: lock driver Or unlock driver when hardware reset (No command or data will be written to driver when the lock is high) [POR=12_{HEX}]
0 0	FE	1 X_7	1 0	1 0	1 0	1 0	1 0	1 0	0 0	Set Clock Enable	X_7= 0: Disable X_7= 1: Enable [POR=00_{HEX}]

7.3.2.Read Command Table

(D/C# = 0, R/W#(WR#) = 1, E=1(RD# = 0) unless specific setting is stated)

D/C	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command	Description
0	00 - FF	X_7	X_6	X_5	0	X_3	X_2	X_1	X_0	Status Register Read	X_7=0: indicates the driver is ready for command. X_7=1: indicates the driver is Busy. X_6=0: indicates normal segment mapping with column address. X_6=1: indicates reverse segment mapping with column address. X_5=0: indicates the display is ON. X_5=1: indicates the display is OFF. $X_3X_2X_1X_0$ = 0010, the 4-bit is fixed to 0010 which could be used to identify as Device.

7.4 Temperature Compensation

Table 7: TC Table

Temperature, T(℃)	View Area Clear Duration (ms)	View Area Idle Duration (ms)	Active Area Clear Duration (ms)	Active Area Idle Duration (ms)	Drive Duration (ms)
50≤T<70	6	12	100	12	6
10≤T<50	18	12	100	12	18
0≤T<10	35	12	150	12	35
-5≤T<0	50	12	200	12	50
-10≤T<-5	80	12	250	12	80
-15≤T<-10	150	12	350	12	150
-20≤T<-15	350	12	700	12	350

8. Optical Characteristics at 25℃

Table 8

Item	Symbol	Value			Unit	Condition	
		Min.	Typ.	Max.			
Image refresh time	-	-	1.8	-	S	VDD=3.0V, VLCD =24V, @25□	
Contrast ratio	CR	-	6	-	-	-	
Optimum viewing area Cr ⩾ 2	θ1(6 o'clock)	-	80	-	DEG	ϕ = 0°	Vop= Optimum voltage
	θ2(12 o'clock)	-	80	-			
	ϕ1(3 o'clock)	-	80	-		ϕ = 0°	
	ϕ2(9 o'clock)	-	80	-			

8.1 Optical Characteristics Definition

8.1.1 Viewing Angle

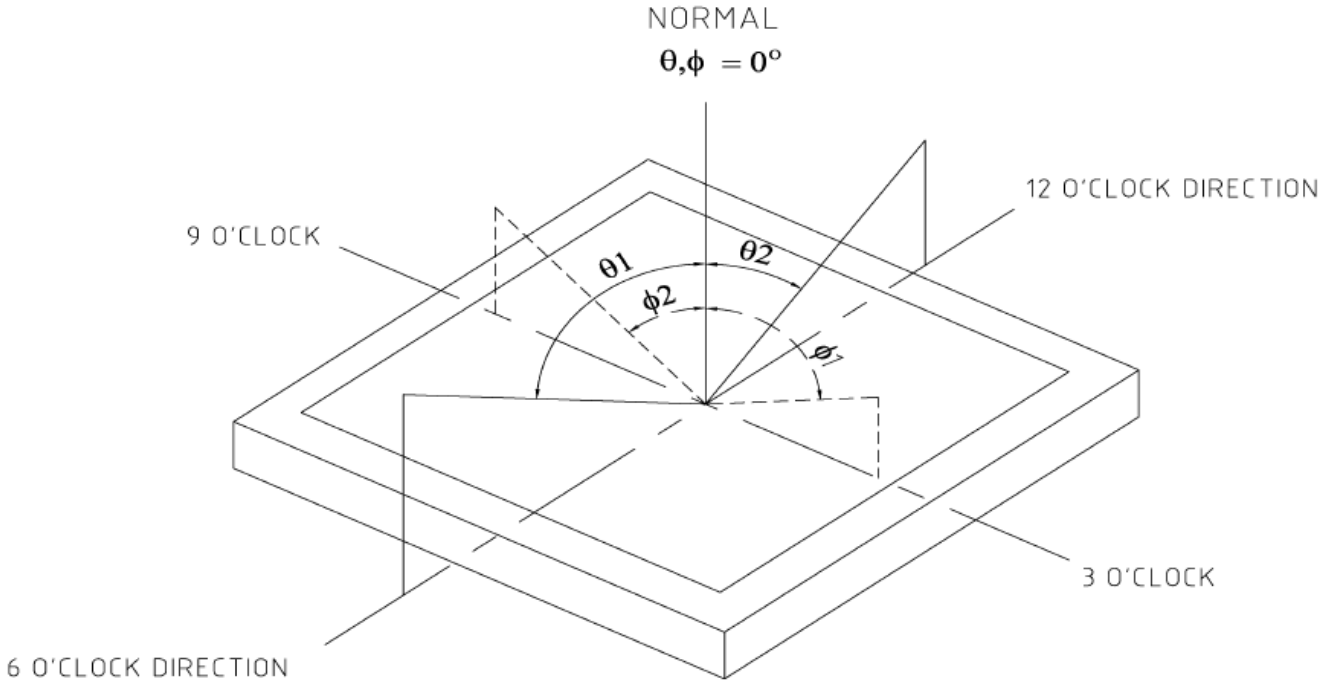


Figure 5

8.1.2 Contrast Ratio

B1 = pixel luminance at stable dark state

B2 = pixel luminance at stable bright state

Contrast Ratio = B2/B1

9. LCD Cosmetic Conditions

LCD size of the product is small.

10. HANDLING PRECAUTION

(1) Mounting Method

The panel of the LCD Module consists of two thin glass plates with polarizers which easily get damaged since the Module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling the LCD Modules.

(2) Caution of LCD handling & cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- Isopropyl alcohol
- Ethyl alcohol
- Trichloro trifloro thane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Ketone
- Aromatics

(3) Caution against static charge

The LCD Module use C-MOS LSI drivers, so we recommend that you connect any unused input terminal to VDD or VSS, do not input any signals before power is turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

(4) Packaging

- Modules use LCD elements, and must be treated as such. Avoid intense shock and falls from a height.
- To prevent modules from degradation. Do not operate or store them exposed directly to sunshine or high temperature/humidity.

(5) Caution for operation

- It is indispensable to drive LCD's within the specified voltage limit since the higher voltage than the limit shorten LCD life. An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them.However those phenomena do not mean malfunction or out of order with LCD's. Which will come back in the specified operating temperature range.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the relative condition of 40°C, 50%RH or less is reequired.

(6) Storage

In the case of storing for a long period of time (for instance.) For years) for the purpose or replacement use, The following ways are recommended.

- Storage in a polyethylene bag with sealed so as not to enter fresh air outside in it, And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping temperature in the specified storage temperature range.
- Storing with no touch on polarizer surface by the anything else. (It is recommended to store them as they have been contained in the inner container at the time of delivery)

(7) Safety

- It is recommendable to crash damaged or unnecessary LCD into pieces and wash off liquid crystal by using solvents such as acetone and ethanol.

Which should be burned up later.

(8) Other

- After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

11. PACKING INSTRUCTION